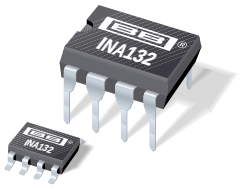
BURR - BROWN®



INA132

Low Power, Single-Supply DIFFERENCE AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 160μA
- WIDE SUPPLY RANGE
  Single Supply: 2.7V to 36V
  Dual Supplies: ±1.35V to ±18V
- LOW GAIN ERROR: ±0.075% max
- LOW NONLINEARITY: 0.001% max
- HIGH CMR: 90dB
- HIGHLY VERSATILE CIRCUIT
- EASY TO USE
- LOW COST
- 8-PIN DIP AND SO-8 PACKAGES

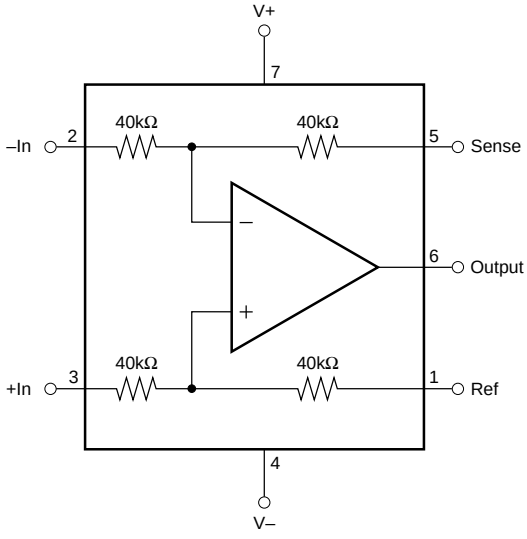
APPLICATIONS

- DIFFERENTIAL INPUT AMPLIFIER
- INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- G = 1/2 AMPLIFIER
- G = 2 AMPLIFIER
- SUMMING AMPLIFIER
- DIFFERENTIAL CURRENT RECEIVER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- BATTERY-POWERED SYSTEMS
- GROUND LOOP ELIMINATOR

DESCRIPTION

The INA132 is a low power, unity-gain differential amplifier consisting of a precision op amp with a precision resistor network. The on-chip resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The internal op amp's common-mode range extends to the negative supply—ideal for single-supply applications. It operates on single (2.7V to 36V) or dual supplies (±1.35V to ±18V).

The differential amplifier is the foundation of many commonly used circuits. The INA132 provides this circuit function without using an expensive precision resistor network. The INA132 is available in 8-pin DIP and SO-8 surface-mount packages and is specified for operation over the extended industrial temperature range, –40°C to +85°C.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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PDS-1353A
Printed in U.S.A. November, 1996

SPECIFICATIONS: $V_S = \pm 15V$

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ connected to Ground, and Reference Pin connected to Ground, unless otherwise noted.

PARAMETER	CONDITIONS	INA132P, U			INA132PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE[1]	RTO							
Initial			±75	±250		✻	±500	µV
vs Temperature			±1	±5		✻	±10[4]	µV/°C
vs Power Supply	V_S = ±1.35V to ±18V		±5	±30		✻	✻	µV/V
vs Time			0.3			✻		µV/mo
INPUT IMPEDANCE[2]								
Differential			80			✻		kΩ
Common-Mode			80			✻		kΩ
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range	V_O = 0V	(V–)		2(V+)–2	✻		✻	V
Common-Mode Rejection	V_{CM} = –15V to 28V, R_S = 0Ω	76	90		70	✻		dB
OUTPUT VOLTAGE NOISE[3]	RTO							
f = 0.1Hz to 10Hz			1.6			✻		µVp-p
f = 1kHz			65			✻		$nV/\sqrt{Hz}$
GAIN								
Initial			1			✻		V/V
Error	V_O = –14V to 13.5V		±0.01	±0.075		✻	±0.1	%
vs Temperature[4]			±1	±10		✻	✻	ppm/°C
vs Nonlinearity	V_O = –14V to 13.5V		±0.0001	±0.001		✻	±0.002	% of FS
OUTPUT								
Voltage, Positive	R_L = 100kΩ to Ground	(V+)–1	(V+)–0.8		✻	✻		V
Negative	R_L = 100kΩ to Ground	(V–)+0.5	(V–)+0.15		✻	✻		V
Positive	R_L = 10kΩ to Ground	(V+)–1.5	(V+)–0.8		✻	✻		V
Negative	R_L = 10kΩ to Ground	(V–)+1	(V–)+0.25		✻	✻		V
Current Limit, Continuous to Common			±12			✻		mA
Capacitive Load (Stable Operation)			10,000			✻		pF
FREQUENCY RESPONSE								
Small Signal Bandwidth	–3dB		300			✻		kHz
Slew Rate			0.1			✻		V/µs
Settling Time: 0.1%	V_O = 10V Step		85			✻		µs
0.01%	V_O = 10V Step		88			✻		µs
Overload Recovery Time	50% Overdrive		7			✻		µs
POWER SUPPLY								
Rated Voltage			±15			✻		V
Voltage Range		±1.35		±18	✻		✻	V
Quiescent Current	I_O = 0mA		±160	±185		✻	✻	µA
TEMPERATURE RANGE								
Specification		–40		+85	✻		✻	°C
Operation		–55		+125	✻		✻	°C
Storage		–55		+125	✻		✻	°C
Thermal Resistance, Θ_{JA}								
8-Pin DIP			100			✻		°C/W
SO-8 Surface-Mount			150			✻		°C/W

✻Specifications the same as INA132P.

NOTES: (1) Includes effects of amplifier's input bias and offset currents. (2) 40kΩ resistors are ratio matched but have ±20% absolute value. (3) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network. (4) Guaranteed by wafer test to 95% confidence level.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

SPECIFICATIONS: V_S = +5V

At T_A = +25°C, V_S = +5V, R_L = 10kΩ connected to V_S/2, and Reference Pin connected to V_S/2, unless otherwise noted.

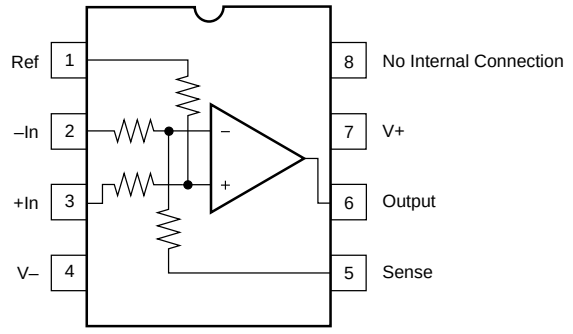
PARAMETER	CONDITIONS	INA132P, U			INA132PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE[1]	RTO							
Initial			±150	±500		✻	±750	µV
vs Temperature			±2			✻		µV/°C
INPUT VOLTAGE RANGE								
Common-Mode Voltage Range		0		2(V+)–2	✻		✻	V
Common-Mode Rejection	V_{CM} = 0V to 8V, R_S = 0Ω	76	90		70	✻		dB
OUTPUT								
Voltage, Positive	R_L = 100kΩ	(V+)–1	(V+)–0.75		✻	✻		V
Negative	R_L = 100kΩ	+0.25	+0.06		✻	✻		V
Positive	R_L = 10kΩ	(V+)–1	(V+)–0.8		✻	✻		V
Negative	R_L = 10kΩ	+0.25	+0.12		✻	✻		V
POWER SUPPLY								
Rated Voltage			+5			✻		V
Voltage Range		+2.7		+36	✻		✻	V
Quiescent Current	I_O = 0mA		±155	±185		✻	✻	µA

✻Specifications the same as INA132P.

NOTE: (1) Include effects of amplifier's input bias and offset currents.

PIN CONFIGURATION

TOP VIEW **DIP/SOIC**



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V–	36V
Input Voltage Range	±80V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

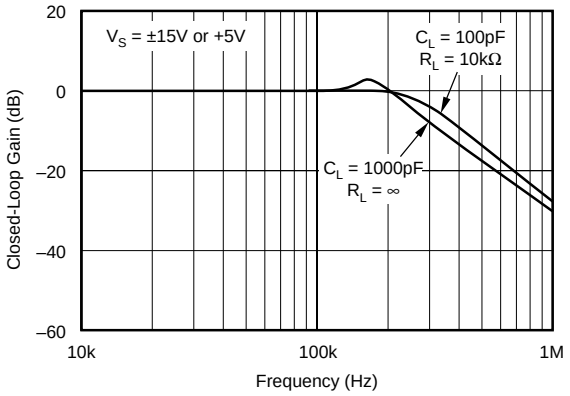
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	TEMPERATURE RANGE
INA132PA	8-Pin Plastic DIP	006	–40°C to +85°C
INA132P	8-Pin Plastic DIP	006	–40°C to +85°C
INA132UA	SO-8 Surface-Mount	182	–40°C to +85°C
INA132U	SO-8 Surface-Mount	182	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

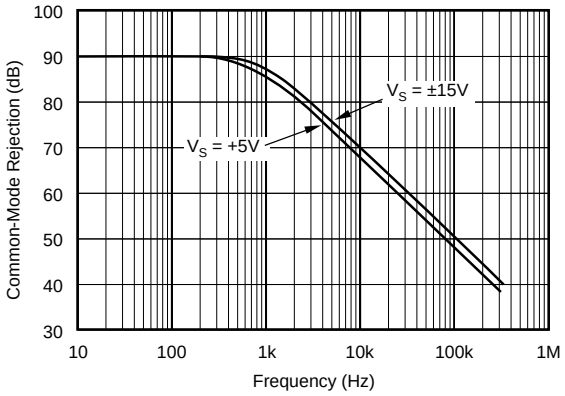
TYPICAL PERFORMANCE CURVES

At T_A = +25°C and V_S = ±15V, unless otherwise noted.

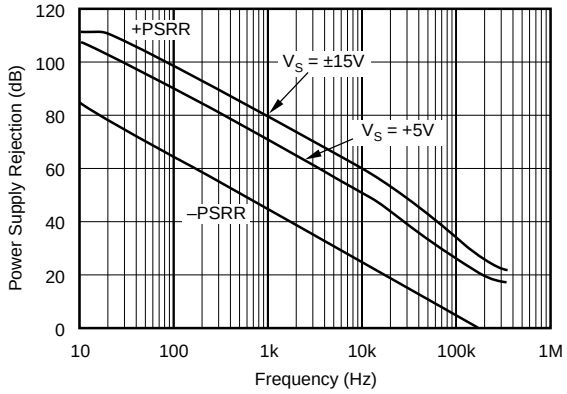
GAIN vs FREQUENCY



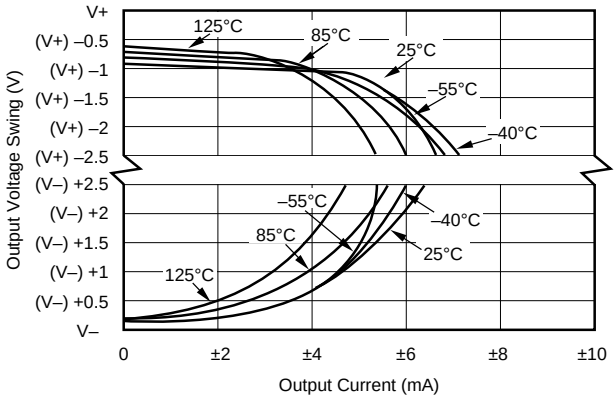
COMMON-MODE REJECTION vs FREQUENCY



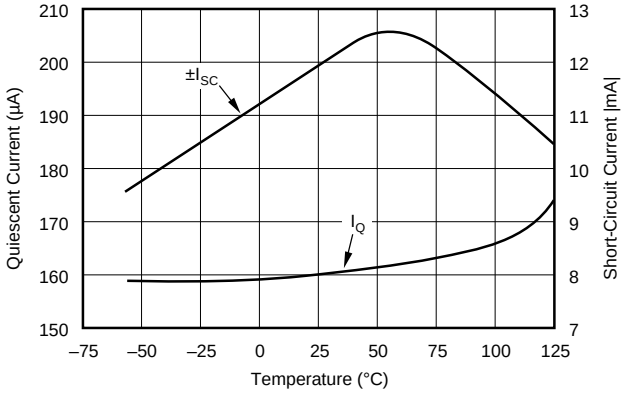
POWER SUPPLY REJECTION vs FREQUENCY



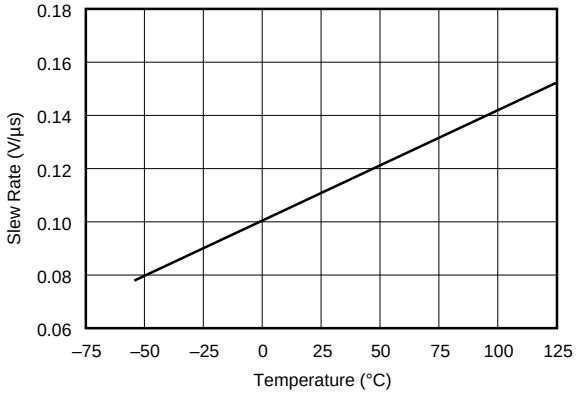
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



QUIESCENT and SHORT-CIRCUIT CURRENT vs TEMPERATURE



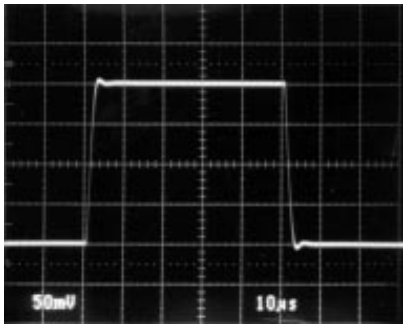
SLEW RATE vs TEMPERATURE



TYPICAL PERFORMANCE CURVES (CONT)

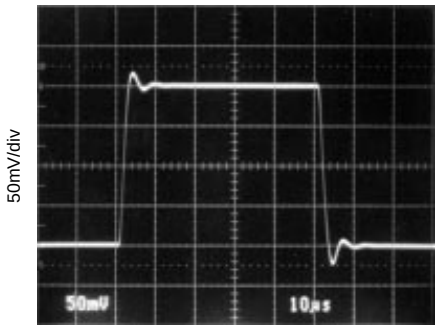
At T_A = +25°C and V_S = ±15V, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE
C_L = 200pF



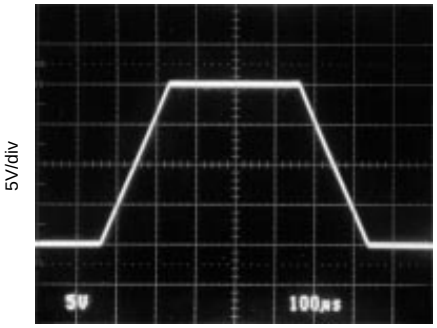
10µs/div

SMALL-SIGNAL STEP RESPONSE
C_L = 1000pF



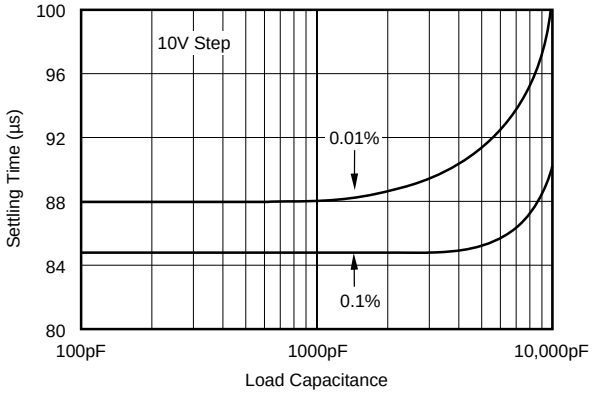
10µs/div

LARGE-SIGNAL STEP RESPONSE

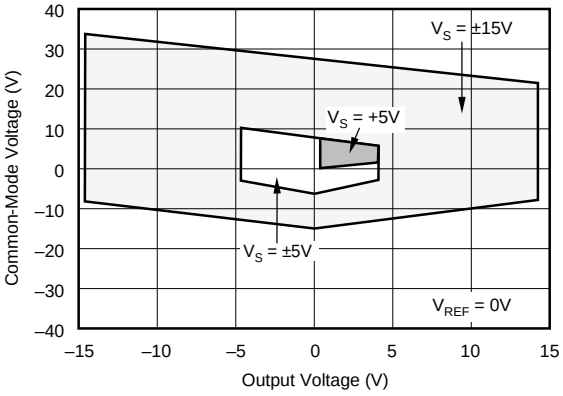


100µs/div

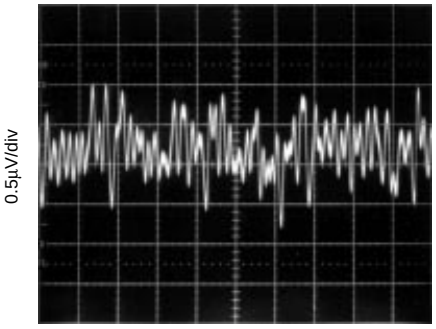
SETTLING TIME vs LOAD CAPACITANCE



INPUT COMMON-MODE VOLTAGE RANGE vs
OUTPUT VOLTAGE



0.1 to 10Hz PEAK-TO-PEAK
VOLTAGE NOISE

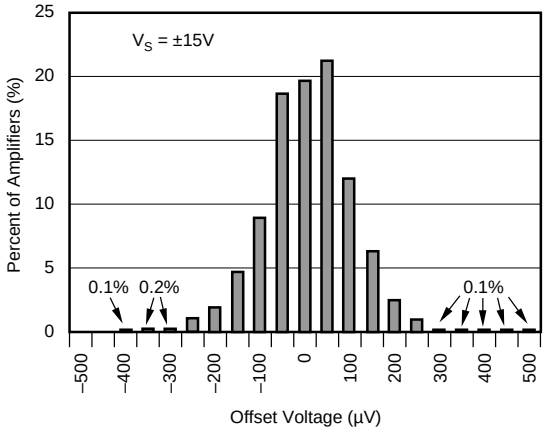


500ms/div

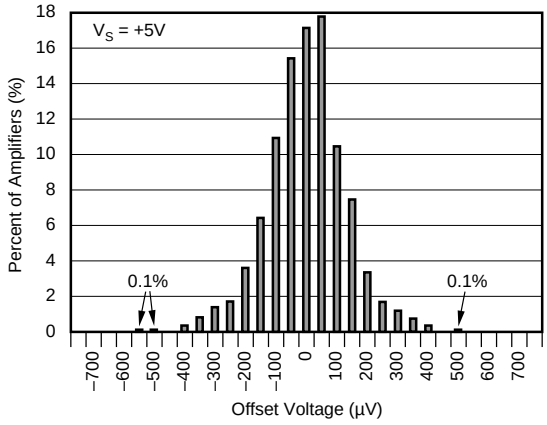
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C and V_S = ±15V, unless otherwise noted.

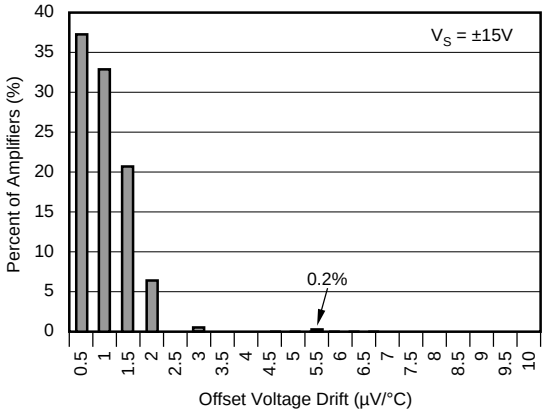
OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA132. Power supply bypass capacitors should be connected close to the device pins.

The differential input signal is connected to pins 2 and 3 as shown. The source impedances connected to the inputs must be nearly equal to assure good common-mode rejection. An 8Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 80dB. Gain accuracy will also be slightly affected. If the source has a known impedance mismatch, an additional resistor in series with one input can be used to preserve good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins would not provide specified performance. As shown in Figure 1, measurements should be sensed at the load.

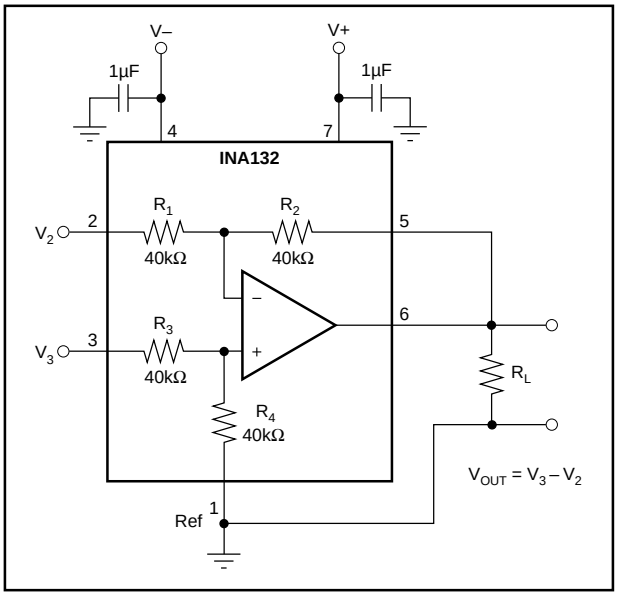


FIGURE 1. Basic Power Supply and Signal Connections.

OPERATING VOLTAGE

The INA132 operates from single (+2.7V to +36V) or dual (±1.35V to ±18V) supplies with excellent performance. Specifications are production tested with +5V and ±15V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

The internal op amp in the INA132 is a single-supply design. This allows linear operation with the op amp's common-mode voltage equal to, or slightly below V– (or single supply ground). Although input voltages on pins 2 and 3 that are below the negative supply voltage will not damage the device, operation in this region is not recommended. Transient conditions at the inverting input terminal below the negative supply can cause a positive feedback condition that could lock the INA132's output to the negative rail.

The INA132 can accurately measure differential signals that are above the positive power supply. Linear common-mode range extends to nearly twice the positive power supply voltage—see typical performance curve, Common-Mode Range vs Output Voltage.

OFFSET VOLTAGE TRIM

The INA132 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage. The source impedance of a signal applied to the Ref terminal should be less than 8Ω to maintain good common-mode rejection. To assure low impedance at the Ref terminal, the trim voltage can be buffered with an op amp, such as the OPA177.

CAPACITIVE LOAD DRIVE CAPABILITY

The INA132 can drive large capacitive loads, even at low supplies. It is stable with a 10,000pF load. Refer to the "Small-Signal Step Response" and "Settling Time vs Load Capacitance" typical performance curves.

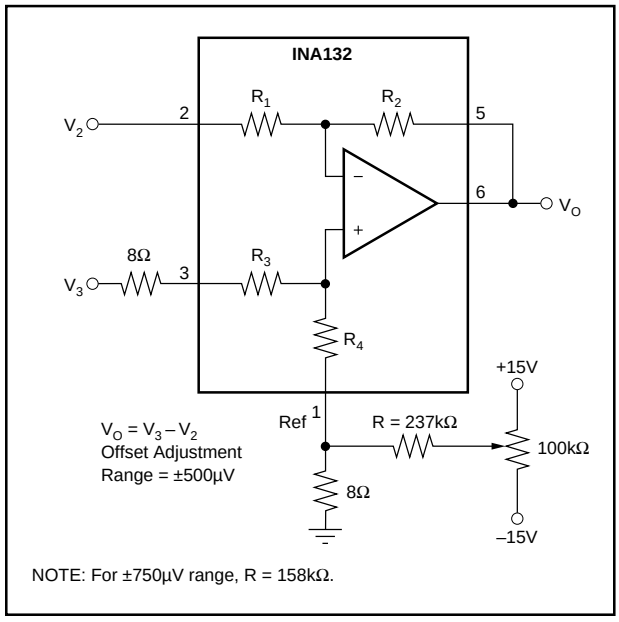
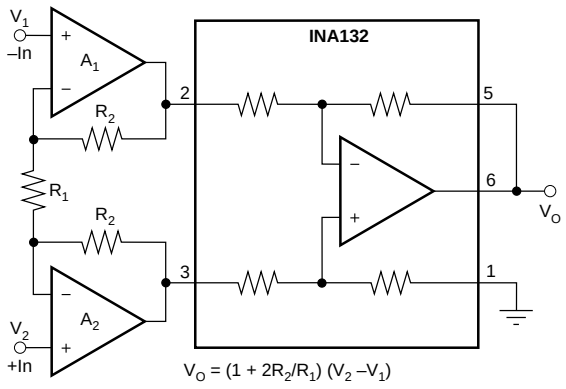


FIGURE 2. Offset Adjustment.



The INA132 can be combined with op amps to form a complete instrumentation amplifier with specialized performance characteristics. Burr-Brown offers many complete high performance IAs. Products with related performances are shown at the right.

A_1, A_2	FEATURE	SIMILIAR COMPLETE BURR-BROWN IA
OPA27	Low Noise	INA103
OPA129	Ultra Low Bias Current (fA)	INA116
OPA177	Low Offset Drift, Low Noise	INA114,INA128
OPA2130	Low Power, FET-Input (pA)	INA111
OPA2234	Single Supply, Precision, Low Power	INA122(1), INA118
OPA2237	Single Supply, Low Power, MSOP-8	INA122(1), INA126(1)

NOTE: (1) Available 1Q'97.

FIGURE 3. Precision Instrumentation Amplifier.

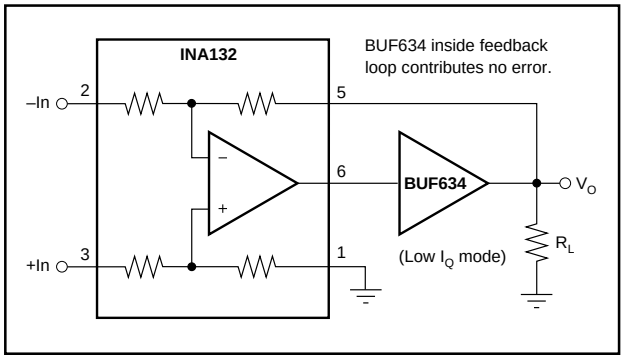


FIGURE 4. Low Power, High Output Current Precision Difference Amplifier.

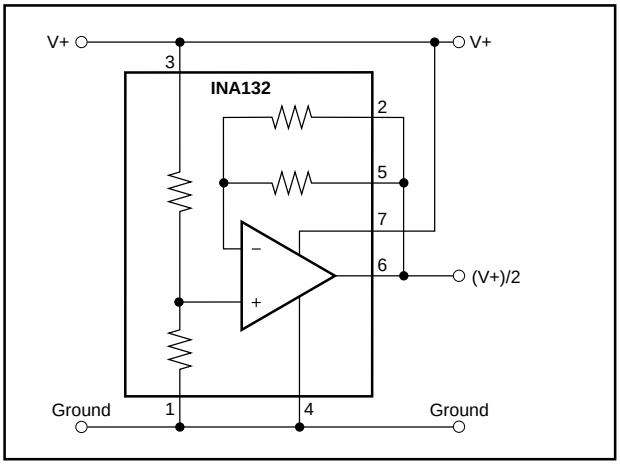


FIGURE 5. Pseudoground Generator.

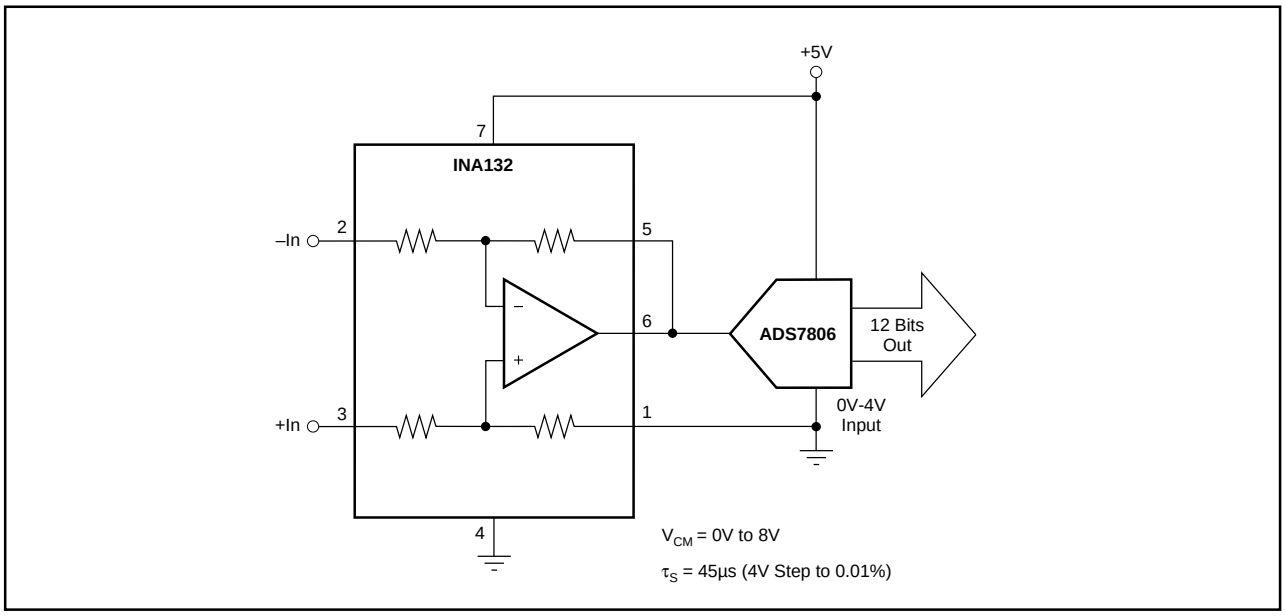


FIGURE 6. Differential Input Data Acquisition.

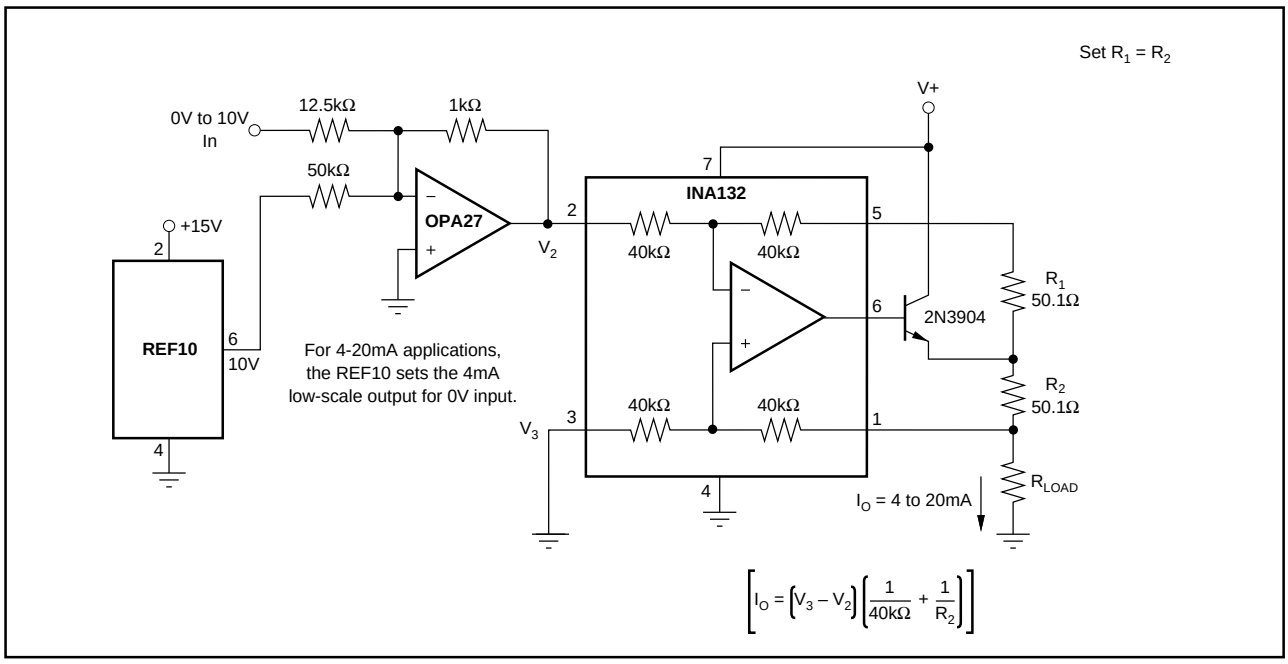


FIGURE 7. Precision Voltage-to-Current Conversion.

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the INA105 data sheet for additional applications ideas, including:

- Current Receiver with Compliance to Rails
- Precision Unity-Gain Inverting Amplifier
- ±10V Precision Voltage Reference
- ±5V Precision Voltage Reference
- Precision Unity-Gain Buffer
- Precision Average Value Amplifier
- Precision G = 2 Amplifier
- Precision Summing Amplifier
- Precision G = 1/2 Amplifier
- Precision Bipolar Offsetting
- Precision Summing Amplifier with Gain
- Instrumentation Amplifier Guard Drive Generator
- Precision Summing Instrumentation Amplifier
- Precision Absolute Value Buffer
- Precision Voltage-to-Current Converter with Differential Inputs
- Differential Input Voltage-to-Current Converter for Low I_{OUT}
- Isolating Current Source
- Differential Output Difference Amplifier
- Isolating Current Source with Buffering Amplifier for Greater Accuracy
- Window Comparator with Window Span and Window Center Inputs
- Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain
- Digitally Controlled Gain of ±1 Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
INA132P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
INA132PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
INA132U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
INA132UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

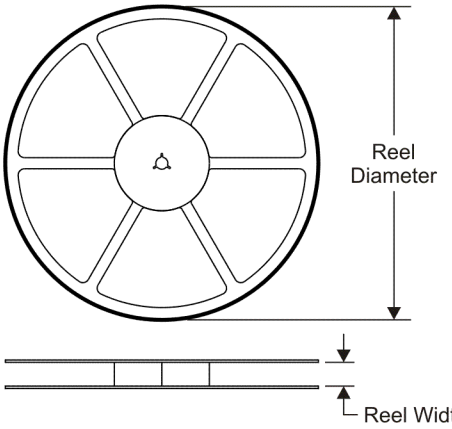
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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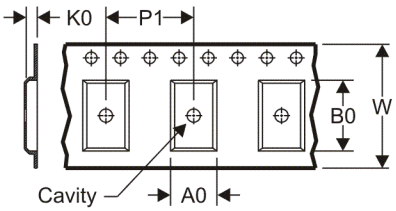
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

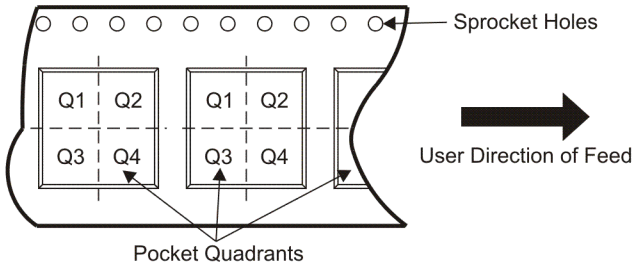


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

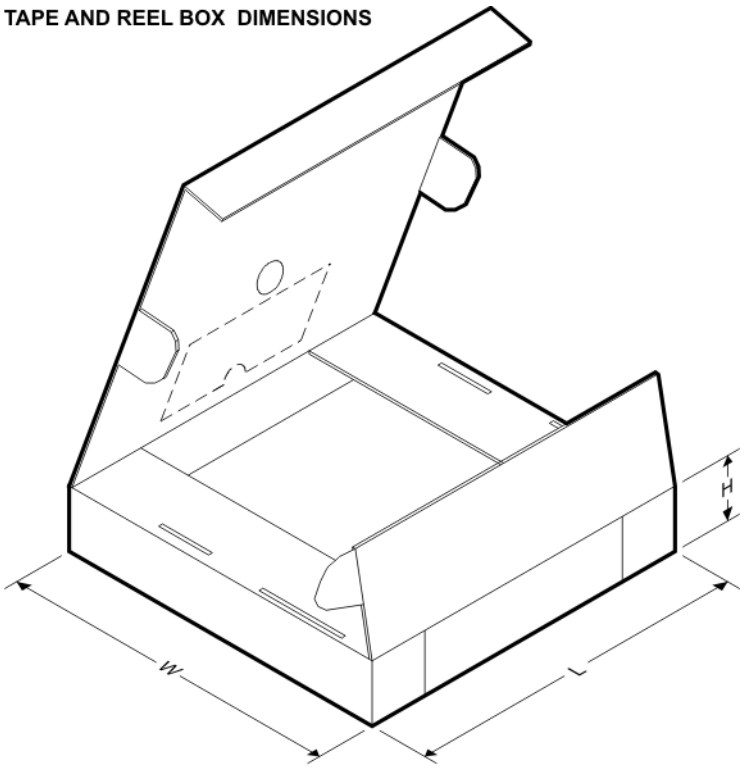
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA132U/2K5	SOIC	D	8	2500	346.0	346.0	29.0
INA132UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0

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